CLAIMS:

1. An apparatus for reducing the memory footprint of a first processor device, the apparatus comprising:

a segment of program code which is split into portions including at least one controlling piece and at least one separate working piece;

a storage area for storing certain pieces of the program code;

a first memory area associated with the first processor device for receiving certain portions of the program code; and

a hardware transfer mechanism for efficiently linking the storage area with the first memory area,

wherein the memory footprint of the first processor device is reduced by locating certain controlling pieces of the program code in the storage area, and transferring only certain working pieces of the program code in the first memory area.

2. The apparatus of Claim 1, wherein the storage area includes a second memory area associated with second processor device.

3. The apparatus of Claim 2, wherein the first processor device includes a high-MIPS processor device having higher-cost memory.

4. The apparatus of Claim 3, wherein the second processor device include a low-MIPS processor device having lower-cost memory.

5. The apparatus of Claim 3, wherein the high-MIPS processor device includes a digital signal processor (DSP) device.

6. The apparatus of Claim 4, wherein the low-MIPS processor device includes a general microcontroller unit (MCU) device.

7. The apparatus of Claim 2, wherein the working piece is further split into code phases and associated data blocks, which are arranged into code and data segments.

8. The apparatus of Claim 7, wherein a store exists in the second memory area for the segments.

9. The apparatus of Claim 8, wherein further included is a segment manager which copies the segments between the store and the first memory area on an as-needed basis.

10. The apparatus of Claim 9, wherein the segment manager utilizes hardware acceleration to achieve efficient transfers.

11. The apparatus of Claim 9, wherein the segment manager is used to schedule segment management from the first processor.

12. The apparatus of Claim 9, wherein the segment manager is used to schedule segment management from the second processor.

13. An method for reducing the memory footprint of a first processor device, the method comprising the steps of:

splitting a segment of program code into portions including at least one controlling piece and at least one separate working piece;

storing certain portions of the program code in a storage area;

receiving certain portions of the program code in a first memory area associated with the first processor device; and

linking the storage area with the first memory area using an efficient hardware transfer mechanism,

wherein the memory footprint of the first processor device is reduced by locating certain controlling pieces of the program code in the storage area, and only certain working pieces of the program code in the first memory area.

14. The method of Claim 13, wherein the storage area includes a second memory area associated with second processor device.

15. The method of Claim 14, wherein the first processor device includes a high-MIPS processor device having higher-cost memory.

16. The method of Claim 15, wherein the second processor device include a low-MIPS processor device having lower-cost memory.

17. The method of Claim 15, wherein the high-MIPS processor device includes a digital signal processor (DSP) device.

18. The method of Claim 16, wherein the low-MIPS processor device includes a general microcontroller unit (MCU) device.

19. The method of Claim 14, wherein the steps further include: splitting the working piece into code phases and associated data blocks, and arranging them into code and data segments.

20. The method of Claim 19, wherein the steps further include creating a store in the second memory area for the segments.

21. The method of Claim 19, wherein the steps further include utilizing a segment manager to copy the segments between the store and the first memory area on an as-needed basis.

22. The method of Claim 21, wherein the segment manager further includes the step of utilizing hardware acceleration to achieve efficient transfers.

23. The method of Claim 21, wherein the steps further include scheduling the segment management; using the segment manager, from the first processor.

24. The method of Claim 21, wherein the steps further include scheduling the segment management, using the segment manager, from the second processor.

25. A distributed signal processing framework for reducing the memory footprint of a digital signal processing device, the framework comprising:

at least one signal processing algorithm, the algorithm being split into a controlling piece and at least one separate processing piece;

a low-MIPS processor device having a high-memory footprint, whereby the controlling piece is stored and runs on the low-MIPS processor device;

a high-MIPS processor having a low-memory footprint, whereby at least one of the separate processing pieces is stored and runs on the high-MIPS processor device; and

a hardware transfer mechanism for efficiently linking the pieces through the distributed framework.

26. A network telephone device, comprising:

a digital signal processing having a cache memory;

an SDRAM; and

a DMA arbiter configured to exchange code and data between the SDRAM and the cache memory.